Design of a silicon charge detector readout system for beam test*

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The High Energy cosmic-Radiation Detection facility (HERD) is a planned experiment on the Chinese Space Station. The Silicon Charge Detector (SCD), one of the sub-detectors in HERD, is used to detect cosmic-ray nuclei with high charge resolution. In this work, we present a compact readout electronics system of SCD that was designed for the HERD heavy ion beam test. It consists of front-end readout electronics with 200 input channels, data acquisition and data management electronics. The test results showed that the SCD readout system had a low noise with a silicon strip detector connected, the dynamic range can be extended from 200 fC to 1200 fC and the cosmic ray test performed as expected.

Keywords: HERD, Silicon charge detector, Readout electronics

I. INTRODUCTION

Cosmic Ray (CR) detection remains in the forefront of intense research and is represented by sophisticated experiments dedicated to the clarification of their origin, acceleration and propagation mechanisms in the Universe [1, 2]. Great insight was obtained from the investigation of CRs over multiple past decades, leading to a deeper understanding of the intrinsic interactions constituting the fields of Particle and Astroparticle Physics. Although important results have been acquired by indirect (ground-based) experiments over the years, there is an imminent need to explore highly energetic CR particles from GeV up to PeV and gamma-rays via direct observations, carried out by space-borne instruments.

The High Energy cosmic Radiation Detector (HERD) is a prominent space-borne instrument to be installed on-board the Chinese Space Station (CSS) around 2027 [3, 4]. The main scientific objectives of HERD include the search for signals of dark matter annihilation products, precise cosmic ray spectrum and composition measurements up to the knee energy, and high energy gamma-ray monitoring and survey [5–7]. The data gathered from the HERD detectors can provide valuable information for developing radiation shielding technologies and mitigating the risks posed by cosmic radiation during long-duration space missions. The HERD project also holds significant implications for fundamental physics research. By studying the properties of cosmic rays, researchers can probe the boundaries of particle physics.

HERD is designed around a segmented, 3-D imaging calorimeter (CALO) [8–11]. Such a design ensures detection of impinging radiation from both its top and 4 lateral sides. Surrounding the calorimeter, a silicon tracker is situated on top active sides above the calorimeter [12]. Subsequently, a Plastic Scintillator Detector (PSD) covering the calorimeter and tracker, will provide gamma-ray and charged particle triggers, together with an additional level of charge measurement [13, 14]. Additionally, further enhancing charge measurement precision, the Silicon Charge Detector (SCD) comprehensively covers all sub-detectors [15]. To effectuate energy calibration of nuclei in the TeV region, a Transition Radiation Detector (TRD) is placed on one of HERD's lateral faces. Consequently, an order of magnitude upgrade in acceptance can be obtained by a novel design with advanced detector techniques fulfilling all physics requirements, while maintaining a manageable payload for a space mission. For the first time, an acceptance > 3 m^2sr for electrons and gamma-rays and of > 2 m^2sr for protons and nuclei will be achieved in a space mission, which will insure the collection of a significative statistics up to the highest energies.

Since silicon strip detector have the characteristics of low noise, good linearity, excellent position and energy resolution, they are widely used in high-energy physics, nuclear physics, and space missions [16–20]. Which is why the SCD is based on several silicon strip detectors. The SCD is the outermost detector of the HERD. The SCD is required to detect the cosmic-ray charge from Z = 1∼28 with resolution typically better than 0.3 c.u. @ Z = 6. In physics, Z refers to the atomic number, and c.u. is used as a unit of measurement of charge, referring to the charge of one electron. The flight configuration of the SCD will consist of five thin detector units. One unit, the SCD placed on the TOP side, active area is a 1.536 × 1.536 m^2 square, while the other units, the SCD situated on the side faces, measure at 1.536 × 0.768 m^2. Each SCD unit consists of eight layers of single-sided silicon strip detectors. The number of silicon strip detectors used for each layer is 256 on the top and 128 on the sides. The total active area of the SCD is approximately 60 m^2. The adjacent layers are installed in orthogonal directions to identify the charge and trajectories of incoming charged particles. This selection ensures a low level of cosmic ray nucleonic fragmentation can be achieved, leading to a decrease in systematic uncertainties while providing a vital charge measurement [21, 22]. Each orthogonal plane pair is composed of a supporting structure made of carbon fiber skins and an aluminum honeycomb core.

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To read out a very large number of detector signals (approximately 500000 channels), we chose an ASIC as the front-end readout chip. A highlight of this work is the expansion of the dynamic range from 200 fC to 1200 fC. To facilitate the detection of particles with Z = 28, we also studied the charge sharing of silicon strip detectors [23]. In order to evaluate the performance of the SCD detectors in the beam test, we developed a set of readout electronics for the SCD prototype. In this study, we will firstly introduce the SCD prototype in brief, and present the detailed design of the readout system. Lastly, the test results will be shown. By analyzing and presenting the test results in detail, we aim to evaluate the performance of the readout system of the SCD prototype.

II. THE SCD PROTOTYPE

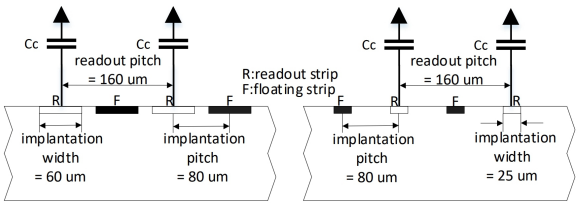


Fig. 1. Layout of the silicon strip sensor

The detector prototype is composed of an AC-coupled single-sided silicon strip detector with an active area of 6 cm $\times$ 3.2 cm, and the thickness is 320 μm. The thickness of the silicon was chosen as a good compromise between the detection efficiency of incident particles that needs high thicknesses and the noise induced by the collection of charges produced by the interaction of the charges that increases with increasing thickness. Fig. 1 illustrates a cross section of the silicon sensor. The surface of the silicon strip detector is a layer of P^+ silicon microstrips covered with a thin aluminum film, with N-type silicon serving as the sensitive area of the detector, and a heavily doped N^+ layer and a backside electrode at the bottom [24]. By applying a sufficiently large reverse voltage to the bar-shaped PN junction, the concentration of drift charge carriers inside becomes very low. At this point, the electric field in the sensitive area approximately follows a linear distribution, and the amount of charge absorbed by the electrode is proportional to the energy deposited by the incident particles [25]. The SCD has 400 implant strips with a pitch of 80 μm. There are two regions with different widths of implant strip, one is 60 μm and the other is 25 μm. Their internal coupling capacitance is 575 pF and 241 pF. The full depletion voltage of SCD is around 30 V and the operating bias voltage is set to 80 V. To reduce the number of the readout channels while maintaining a satisfactory performance in terms of spatial and charge resolution the readout is performed with the so called floating strip approach, where a certain number of the implanted strips are not read out [26, 27]. When high-energy particles hit the silicon strip detector and interact with the sensitive area, the deposited energy generates electron-hole pairs. Under the influence of the external electric field, the electrons and holes drift in two directions, and the silicon stripes rapidly collect charge information. The charge information will be used to infer the trajectory and energy of the incident particle [28, 29]. In the HERD project, multiple silicon strip detectors will be cascaded into an array to increase the detection area [30, 31].

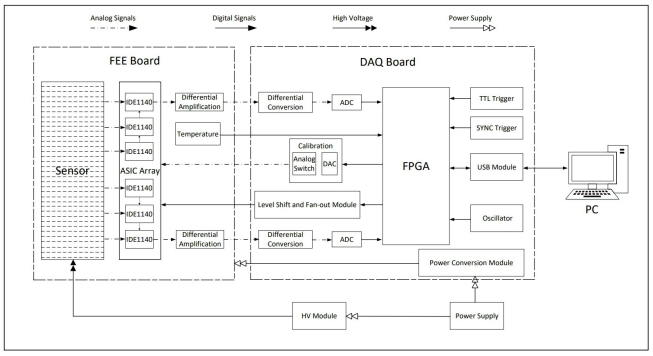


Fig. 2. Structure of the electronic system

To achieve low power consumption and high integration, the electronics of the prototype is divided into two parts: the front-end readout electronics (FEE) and the back-end data acquisition (DAQ), as shown in Fig. 2.

The FEE board comprises an silicon strip detector, two sets of ASIC arrays, two sets of differential amplification circuits, and a temperature acquisition module. Three ASICs are cascaded into an array to amplify and read out the charge signals from the SCD. The differential amplification circuits process the differential analog current signals outputted by the ASIC array before they enter the DAQ board. Temperature changes affect the detector's performance. Generally, as temperature rises, the resistivity of silicon decreases, and the rate of generation of carriers increases, which may lead to increased noise or decreased sensitivity of the detector. It is necessary to measure the temperature and analyze the relationship between temperature and performance.

The DAQ board consists of two sets of differential conversion modules, two sets of ADC modules, calibration modules, ASIC control signal level conversion and fan-out modules, an FPGA, TTL trigger modules, synchronous trigger modules, USB modules, power conversion modules, and high-voltage modules. Acting as the central processing unit, the FPGA governs the entire electronic system, receiving and relaying commands from the host computer, packaging scientific data and then transmitting them to the host computer.

The SCD and charge sensitive preamplifier IDE1140 which produced by IDEAS are bonded to the FEE circuit board using conductive adhesive [32]. Employing a fully automated wire bonding machine, the pins of SCD and IDE1140 are wire-bonded to the solder pads on the PCB to establish electrical connections. The dimensions of the unpackaged die IDE1140 are 6.5 mm $\times$ 6.2 mm, with 64 wires to be laid out within the 6.2 mm width of the chip. The spacing between adjacent wires is less than 100 μm, balancing the processing

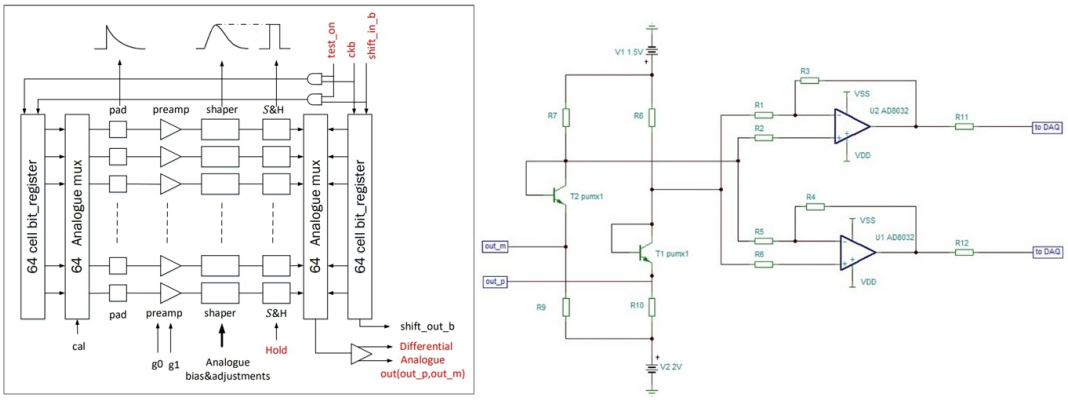


Fig. 3. a Internal architecture of the IDE1140. b Differential amplification circuit

difficulty of the PCB and the robustness of the bonding. The solder pads utilize a chemical nickel-palladium-gold process to prevent oxidation, enhancing the stability of wire bonding.

The silicon detector section requires shading protection, and the entire FEE board needs to be sealed inside a shielding enclosure. A shielding enclosure has been designed for the FEE, with a carbon fiber exterior. This design achieves both protection and light shielding. Moreover, carbon fiber has a low mass-to-weight ratio, ensuring minimal impact on incident radiation. During beam experiments, the beam will strike a fixed area of the silicon detector. To reduce mass, the backside of the silicon detector on the FEE is hollowed out.

The following sections will provide a detailed introduction to the design of the FEE and DAQ. Besides, a minimum front-end readout board (miniFEE) was designed to test dynamic range and load noise. Only one ASIC is wire-bonded on the miniFEE board, without silicon detectors.

III. THE DESIGN OF THE FRONT-END

The main function of FEE is to amplify the analog signal detected by the silicon strip detector. The FEE is composed of two ASIC arrays and differential amplification circuits, as shown on the left of Fig. 2.

Considering the dynamic range, noise level and power consumption, IDE1140 is selected as the front-end readout chip. This chip has 64 readout channels, large dynamic range (-200 fc to +200 fc), low noise (139 e^- for 0 pF input), and low power consumption (0.29 mW/channel). This chip implement 64 parallel charge sensitive preamplifier (CSA) and shaper circuit, with multiplexed analog readout, calibration facilities, and internally generated biases [33]. The pulse height from all channels can be sampled simultaneously and switched via an analog multiplexer to one differential analog current output buffer. In the FEE, three IDE1140 chips are connected in a daisy-chain.

Fig. 3a shows the architecture of IDE1140 [34]. The normal mode and test mode of IDE1140 can be controlled externally by a "test_on" signal. The normal mode is that the 64 inputs are connected to a sensor, which delivers electrical charges to the pre-amplifier inputs. In test mode, it is not necessary to connect any sensor. This mode connects the pulse input generated by the DAC circuit to the cal pad via a switch controlled by the bit-register. Also, in this case, only one channel can be calibrated at the same time. The chip includes a 2 pF calibration capacitor for testing. When an electron-hole pair is formed in the silicon detector, the charge signals are injected into the corresponding IDE1140 input channel. These signals are amplified by the CSA, and then pass through a slow shaper circuit to broaden the signal peak, forming a Gaussian-like signal. The "hold" signal is used to control the sample-and-hold circuit, which holds and samples the Gaussian-like signal at its peak by setting a proper hold time. Usually, after the peak is reached (6.5 μs), an external "hold" signal should be applied to sample the value. 64 channel's outputs can be switched in the multiplexer that is controlled by a bit-register. The "shift_in_b" and "ckb" signals are used to control the bit-register, which can perform a sequential read-out. The multiplexer output is buffered and can be read out at the signals "outp" and "outm". Only one of the switches in the mux can be "on" at a time, meaning that the chip's output can only display one channel at a time. The logic part of the chip can be reset either by applying the "dreset" or, simply by running through a normal read-out once.

The differential current signals from the ASIC are amplified and converted to a pair of differential voltage signals by the differential amplification circuit as shown in Fig. 3b. The differential current signals outputted by the ASIC are individually directed into a transistor, converting the current signals into voltage signals. Subsequently, they enter differential amplification circuits where the signals are amplified to fit within the voltage range of the ADC, maximizing the utilization of the ADC's dynamic range. Decreasing the resistance values of the feedback resistors R3 and R4 can diminish the gain of the front-end circuit, thereby expanding the measurement's dynamic range. During signal transmission, signal lines may encounter electromagnetic interference or other external disturbances, resulting in additional common noise on the sig-

nal lines. The utilization of differential amplification circuits aids in reducing common noise caused by factors such as poor grounding and power supply.

IV. BACK-END DATA ACQUISITION AND CONTROL SYSTEM

A. DAQ design

The input of the DAQ requires connection to a silicon charge detector the scientific data output rate is 10 Mbps, and the external trigger enters the DAQ through an I^2C interface. The analog–to–digital conversion, the data packaging, the charge inject function as well as the data transmission are all done by DAQ. The DAQ board includes an FPGA, ADC module, calibration module, trigger module, USB communication module, and power supply module. Xilinx's FPGA chip XC3S500E has been selected as the main control chip. The ADC chip is the AD7476 with a 12-bit serial output, which has a throughput rate of 1 MSPS and power consumption of only 3.6 mW [35]. This ADC chip ensures high precision and efficiency in converting analog signals to digital data. For USB communication, the DAQ system relies on the Cypress CY7C68013A chip. This selection is made based on its suitability for USB interfacing tasks, providing reliable and high-speed communication between the DAQ board and the host computer. Using this chip ensures the timely and accurate transfer of experimental data for further analysis and processing.

The DAQ operation logic consists of four modes: self-triggering mode, calibration mode, synchronous external triggering mode, and TTL external triggering mode. The self-triggering mode uses a 50 Hz periodic signal generated by the FPGA as the internal trigger source. This mode tests the system for proper operation and acquires pedestal data through multiple events. The calibration mode uses a 10 kHz trigger signal generated by the FPGA to calibrate the range of the measured charge in the system, determining the linearity of the system. The FPGA controls the IDE1140 to select the test mode. The host system permits the adjustment of calibration pulses with amplitudes ranging from 0 V to 2 V. These commands are decoded and forwarded to the FPGA via USB. Subsequently, the FPGA is responsible for configuring the parameters of the calibration circuit. There are two trig modes for both the standalone test and the beam test. For the standalone test, a simple TTL signal is enough. The external +3.3 V trigger signal can be directly inputted to the FPGA through an SMA connector. For the beam test, the trig signal from the trigger system with I^2C protocol was used, which included the trigger number, and trigger type, ensuring accurate synchronization and control.

The analog-to-digital conversion circuit is responsible for digitizing the differential signals outputted by the front-end electronics and transmitting the data to the FPGA unit. Initially, the differential signals from the front-end electronics are converted into single-ended signals using an operational amplifier. Subsequently, the converted signals are digitized

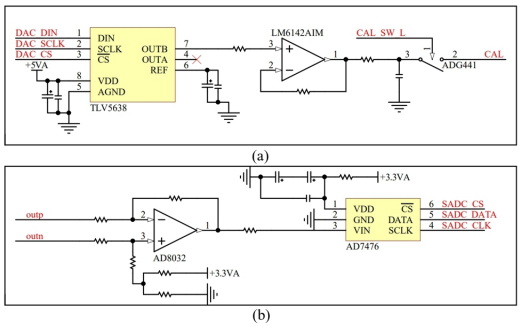


Fig. 4. a Analog-to-digital conversion circuit. b Calibration circuit

using a 12-bit serial ADC chip, AD7476, as shown in Fig. 4a. Biasing is applied to the operational amplifier during the conversion of differential signals to single-ended signals, ensuring that the converted signals fall within the suitable ADC dynamic range. The sliding resistor can adjust the pedestal. The DAQ board has two sets of differential conversion circuits and ADCs, each set corresponding to 3 IDE1140 chips. The utilization of the serial ADC chip AD7476 primarily stems from considerations regarding power consumption. Given that the total number of readout channels in the SCD is approximately 500000, necessitating 1500 ADC chips, the power consumption of each ADC chip significantly impacts the overall system power consumption. Hence, the AD7476, with a power consumption of merely 3.6 mW (at a sampling rate of 1 MSPS with a +3 V power supply), was selected for its low power consumption characteristics.

As depicted in Fig. 4b, the calibration circuit is utilized to inject pulses of varying amplitudes into IDE1140 during test mode [36]. During system testing, a stable level is initially outputted by the serial DAC chip TLV5638 to adjust the amplitude of the pulse signal [37]. The output voltage of TLV5638 remains linear within the range of 0-2 V, effectively covering the dynamic range of IDE1140. Subsequently, pulse signals are generated by the opening and closing of the analog switch ADG441. The step pulse signal is input to the calibration pin of the IDE1140. A first-stage buffer has been interposed between the serial DAC and the analog switch to enhance the signal-driving capability. Through the 2 pF coupling capacitor integrated with the IDE1140, the calibration circuit simulates external charge injection. Only one channel can be calibrated at the same time. By changing the analog switch and "ckb" signal sequentially, all the channels can be tested.

The scientific data packet includes a packet header, 384 channels of ADC values, temperature value, version number, trigger ID, trigger type, trigger sequence number, and packet end. The data packet is 512 $\times$ 16 bits in length and is stored in the FIFO of the FPGA.

The FPGA logic design corresponds to hardware functionalities, primarily comprising main control logic, reset and clock management, IDE1140 control, ADC control, calibration pulse generation, trigger management, and USB communication. The main control logic decodes commands received from the USB communication module, including commands

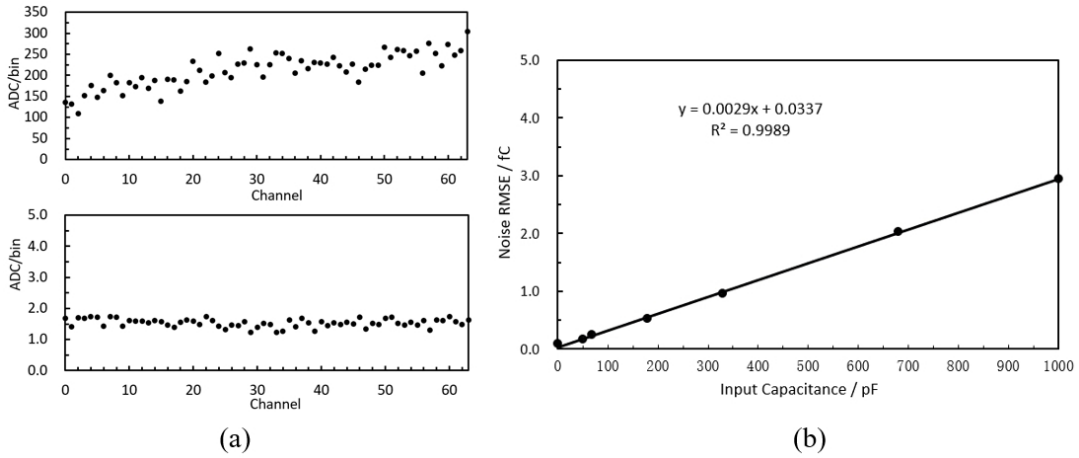


Fig. 5. a 64 channels of pedestal and RMSE without detector. b Noise slope curve of the IDE1140

for setting operational modes, selecting trigger sources, configuring trigger acquisition delay, and setting DAC output amplitudes. The reset and clock management logic is responsible for generating the system's reset signal and the clock signals for various sub-modules. When the system is powered on, the reset signal is set to a low level and the system is reset. After 10 μs of power-on, the reset signal becomes high level, indicating that the system has entered a waiting state. The clock management module primarily utilizes the FPGA's internal Digital Clock Manager (DCM) to correct clock offsets, adjust clock phases, reconfigure input clock division, and integrate the processed clock into the global clock network. In this design, the input clock is generated by an external high-precision crystal oscillator with a frequency of 20 MHz. The IDE1140 control logic encompasses two sub-modules that generate the IDE1140 control signal timing for normal mode and test mode. The ADC control logic generates control logic for single analog-to-digital conversions as per device specifications, receives serial data from the ADC and writes digitized data into FIFO buffers. The ADC driver is implemented with a state machine, using a 20 MHz global clock "clk" as the driver signal. The entire conversion process requires 16 clock cycles to complete (0.8 microsec). On the falling edge of the 16th clock signal, ADC returns to the initial state to convert the data of the next channel. The calibration pulse generation logic comprises two sub-modules: DAC control logic and analog switch control logic. The voltage level of the DAC output is configured by the main control module. The analog switch control logic operates during the internal electronic calibration period. The injection of calibration signals is accomplished by generating high-speed pulse signals through the use of fast-switching simulated switches. The timing intervals between channel selection and pulse injection, as well as pulse widths, are controlled by counters.

V. PERFORMANCE OF THE READOUT SYSTEM

The mini-FEE board was first designed to facilitate testing of the single-channel pedestal and noise. The FEE board was also designed to participate in the beam test at CERN in 2022.

We performed the pedestal and noise of the system with no signal input. We also studied the noise level of the electronic system under different capacitance loads.

In addition, we performed energy calibration to test the performance of the electronic system. Simulate the circuit of the acquisition system to calculate the dynamic range of the electronic system. Perform internal calibration and external injection tests on the electronic system, and compare the results of both tests with the simulation result.

A cosmic ray muon test system was built in the laboratory to investigate the performance of the readout system for detecting Minimum ionizing particles (MIPs).

A. Pedestal and noise of miniFEE

In readout electronics, the preamplifier noise has the greatest impact, which can be given by the sum of two components: the intrinsic noise of the preamplifier (noise generated by the electronics without connecting to the silicon detector) and the load noise (defined as the increase in electronic noise when 1 pF capacitance is added to the input).

The mini-FEE board includes the most basic readout circuit. Only one IDE1140 can read out 64 channels of data completely. Capacitors are placed close to the ASIC input pin to reduce the impact of noise.

Using the mini-FEE acquires a pedestal in a certain channel without connecting the detector. The pedestal and the Root Mean Square Error (RMSE) can be achieved by performing Gaussian fitting on the periodic trigger data. As shown in Fig. 5a, We measured 64 channels with pedestal range from 100 to 300 ADC and the RMSE is less than 1.7 ADC (670 e^-).

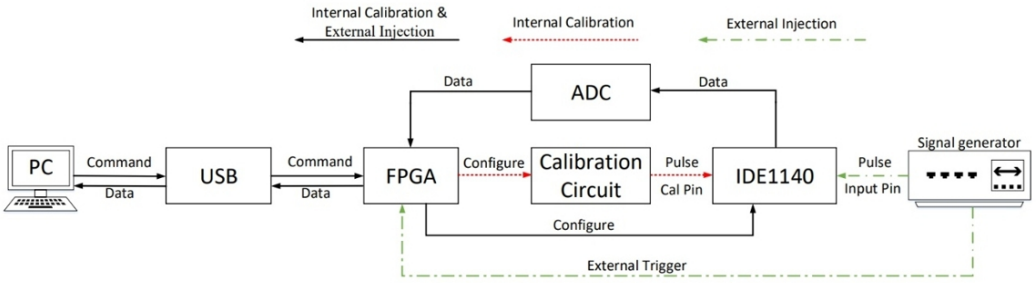
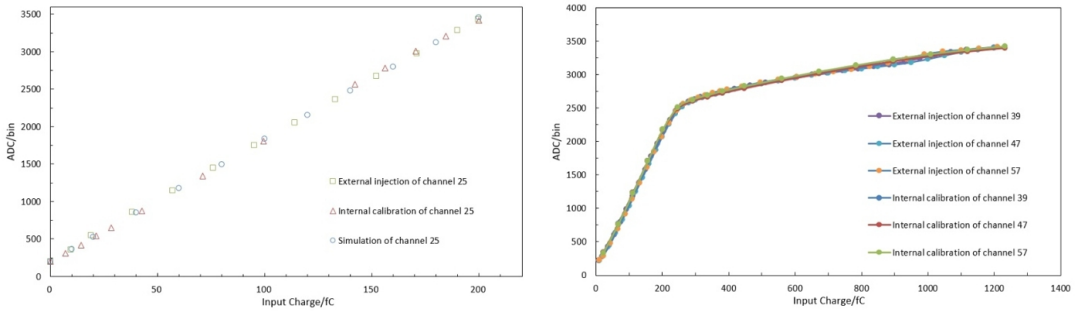


Fig. 6. Schematic diagram of internal calibration and external injection



(a) (b)

Fig. 7. a Test results of the gain ratio using three methods. b Internal calibration and external injection results for three channels

To study the noise level of the readout system under large-area silicon strip detectors, different load capacitances (0 – 1000 pF) were mounted between the input channel 25 to the ground. The noise slope curve of the IDE1140 is shown in Fig. 5b. The equivalent noise charge with a capacitive load of 51 pF is 1034 e^- (0.166 fC). To measure the noise for 0 pF load, the input is connected to the ground. Approximately 10000 events were acquired, the noise is 573 e^- (0.092 fC).

B. Dynamic range and linearity of miniFEE

The chip manual for IDE1140 indicates that the gain in the linear region is 2.6 uA/fC. By simulating the acquisition circuit in TINA, the gain is set to 0.061 fC/bin.

As shown in Fig. 6, perform internal calibration testing of the electronic system in test mode. FPGA controls the calibration circuit as shown in Fig. 4b to inject specified amplitude voltage pulse signals into the calibration pin of IDE1140. These signals are then converted into charge signals by the 2 pF internal coupling capacitors of the ASIC chip. Approximately 10000 events were acquired and the certain channel internal calibration result is shown in Fig. 7a. The gain of the internal calibration is 0.062 fC/bin.

As shown in Fig. 6c, perform external injection testing of the electronic system in normal mode. Using a signal generator to produce a square wave with an amplitude of 0-100 mV and inject it into a certain channel. The rising edge of this square wave is used as the external trigger. Based on Fig. 7a, the external injection gain for a certain channel is 0.065 fC/bin.

By comparing the circuit simulation, internal calibration, and external injection results, the electronic system has good linearity in the range of 0-200 fC, and the integral non-linearity all less than 3%. Furthermore, the relative error of linear fitting for the three test results is less than 1%.

During testing, it was found that the dynamic range of the ASIC is greater than 200 fC. To test the maximum dynamic range of the ASIC, we have modify the gain of the differential amplification circuit as shown in Fig. 3b, and perform internal calibration and external injection tests on the three channels using the same testing method as shown in Fig. 6. The results are shown in Fig. 7b, the linear range is roughly 0-200 fC, consistent with the manual. In the case of ASIC saturation, as the input charge increases, the impedance of the preamplifier becomes larger, leading to a decrease in gain. We observed that the gain decrease when the input charge over 300 fC. After adjustment, the dynamic range can be extended to 1200 fC. In future experiments, it may be necessary to adjust the dynamic range of the silicon strip detector readout system from 200 fC to a larger range.

C. Cosmic-ray test of FEE

The readout system participated in the 2022 CERN beam test. The silicon strip detector designed for the beam test is shown on the left of Fig. 8. It consists of 400 parallel P^+

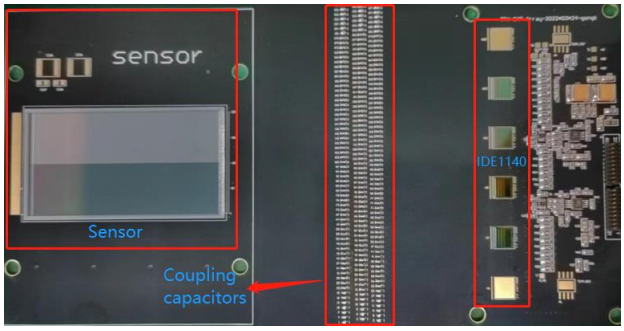


Fig. 8. FEE board

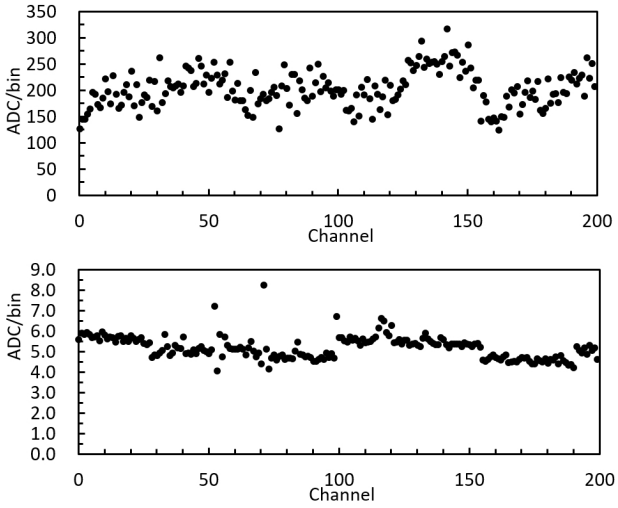


Fig. 9. 200 channels of pedestal and RMSE with detector

strips with a thickness of 320 μm. 200 readout channels are connected to the silicon strips, and 4 ASICs are wire-bonded.

The readout system used a periodic self-trigger to obtain the pedestal and noise. The test results are shown in Fig. 9. It can be observed that the pedestal values of the channels with the detector connected range from 120 to 320 ADC. The RMSE values of the channels are around 5.5 ADC (0.341 fC).

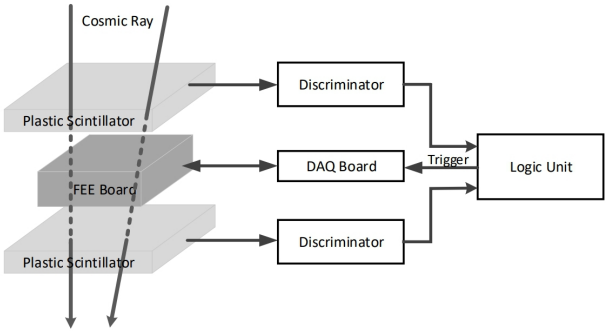


Fig. 10. Block diagram of cosmic ray test system

A cosmic ray test system was also applied to test the performance of the detector for the minimum ionizing particles (MIPs), as shown in Fig. 10. Two plastic scintillators are placed above and below the detector. The size of the plastic scintillators were 12 $\times$ 12 $\times$ 1 cm^3, which is bigger than the SCD. Therefore, most signals were baseline. The cosmic-rays passing through the upper and lower layers of the plastic scintillator simultaneously will be used as trigger signals to initiate data acquisition of the FEE. Theoretically, the energy distribution of cosmic ray follows a Landau distribution. The spectra were fitted with a Landau convoluted Gaussian function.

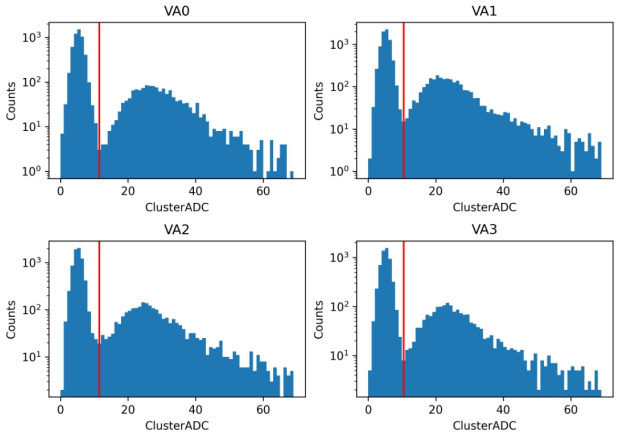


Fig. 11. Cosmic ray spectrum for 4 ASICs

One muon will produce a most probable value of 23000 e^-h^+ pairs in a 320-μm-thick silicon detector. This readout system shows a gain of 15.4 bin/fC as calculated from a linearity test. Through the analysis of long-term cosmic ray test data, the spectrum can be achieved, as shown in Fig. 11. The red lines on the figure represent the threshold (at 3 RMSE). The most probable parameter of Landau density was located at approximately 33 ADC. The response uniformity of the 4 ASICs is good.

VI. CONCLUSION

The project has successfully developed a silicon strip detector readout system, including the FEE and DAQ. The readout system has 384 channels, with 2 watts of power consumption. This detector can measure 200 strip channels simultaneously at a range of 0 to 200 fC with 0.341 fC RMS noise. After adjustment, the dynamic range of this readout system can be extended to 1200 fC. In future experiments, it may be necessary to adjust the dynamic range from 200 fC to a larger range. We have analyzed the beam test data using the new algorithm, and the charge resolution of proton and carbon is approximately 0.10 and 0.20 c.u. on average using the novel algorithm [38]. The results indicate that the readout system has low noise and high resolution, meeting the detection requirements for high-energy cosmic rays.

In future research, we need to perform more detailed energy calibration for a dynamic range of 1200 fC and verify whether this method can be used for charge sharing. Addi-

tionally, this readout system is designed for beam test experiments to validate the key basic circuits. The next step will be to design a more complex and complete SCD electronics system with more readout channels based on this research.

VII. BIBLIOGRAPHY

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